CPE 470 - Open Source IP

RISC V Review

Glossary

ISA: Instruction Set Architecture

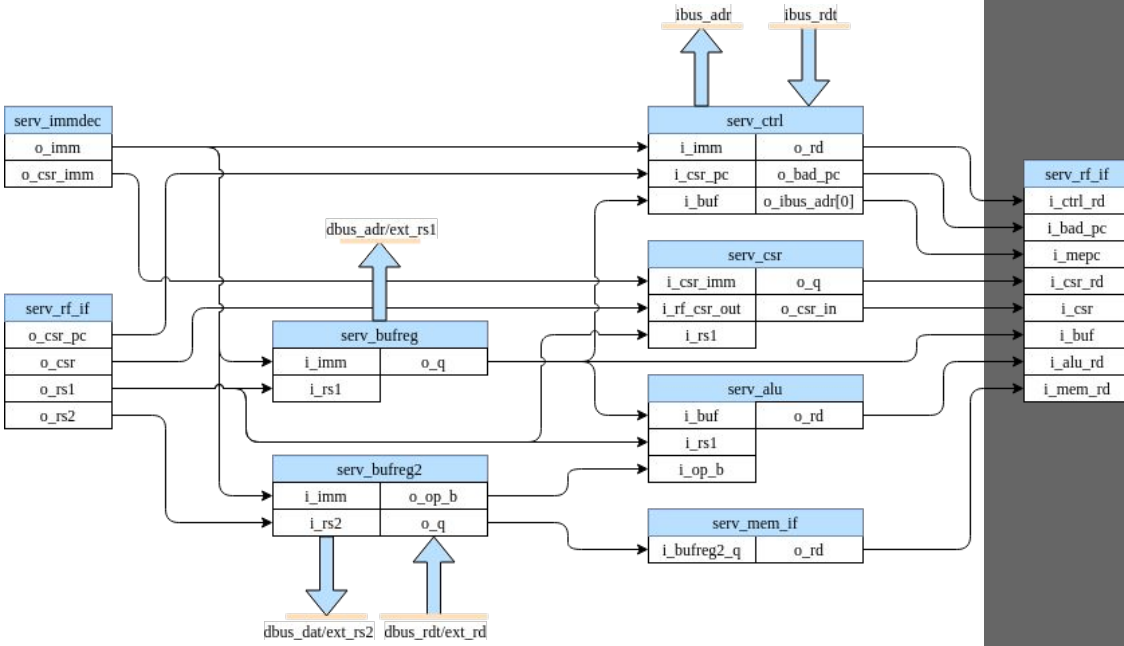
- Base **ISA**s: RV32 or RV64
  - I or E: I has 32 registers, E has 16
  - M: Multiply
  - A: Atomic
  - F: Floating Point
  - D: Double-Precision Floats
  - Zicsr: Control & Status Registers, Interrupts
  - Zifencei: memory ordering protection
  - G: All of the above ^
  - B: Bit Manipulation
  - C: Compressed
- Coprocessors: used to extend ISA, handle unknown instructions
  - Example: send multiply instructions to separate multiplication coprocessor

SERV

- RISC-V RV32I + Fence
  - Optionally: Multiply, Compressed

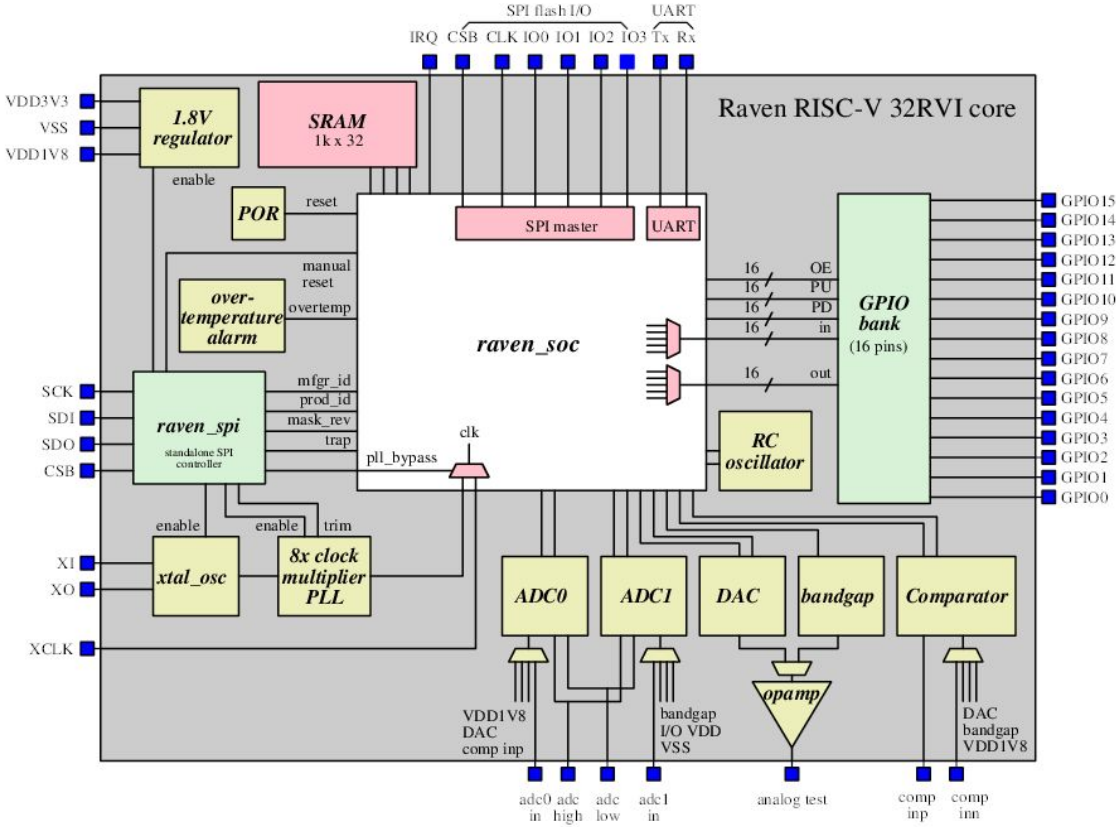
- Smallest RISC V Core
  - 164 flip flops, excluding RF
- One Bit Data Path
  - 32-Bit Add takes 32 cycles
  - 1-bit wide ALU ops
- Coprocessor Support
  - Offloads unknown instructions to extension coprocessors
  - Many SERVs can share one coprocessor, ie. Multiply Unit
- Larger versions available
  - QERV with 4-bit path

- Built by Olof Kindgren
  - Written in Verilog



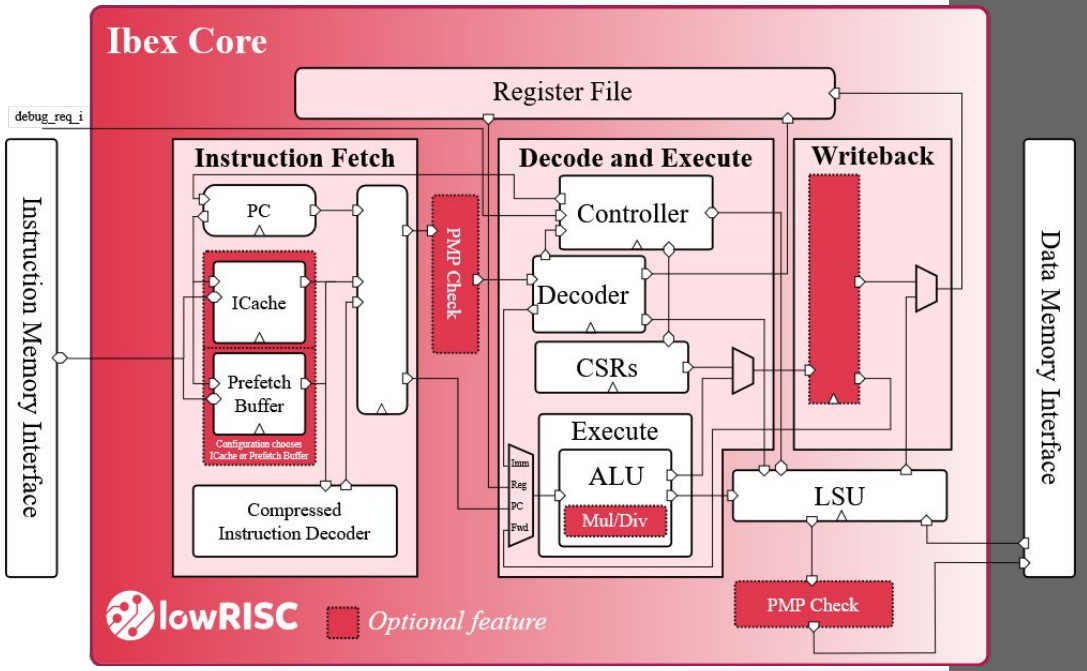
PicoRV32

- RV32I or E
  - Optionally: Multiply, Compressed
  - Multicycle, not pipelined
- Roughly 600 flip flops
  - Size Optimized
- AXI-style interfaces on memory
  - Ready/Valid
- Coprocessor Support
  - “PCPI”
- Built by Yosys / Claire Wolfe
  - Written in Verilog
- Implemented as SoC on Skywater, called Raven



Ibex

- RV32I or E
  - Optionally: Multiply, Compressed, and Bit Manipulation
- Roughly 10 times bigger than SERV
  - ~1000 Flip Flops
- 2 Stage Pipeline
  - Optional 3rd Stage
- Developed by lowRISC and PULP team at ETH Zürich
  - Written in System Verilog



Chipyard - Berkeley IP

- Collection of IP blocks and generation tools for connecting them
- Based on Chisel Language
  - Higher-level HDL based on Scala (Java Family)
  - Chisel gets built into verilog or system verilog
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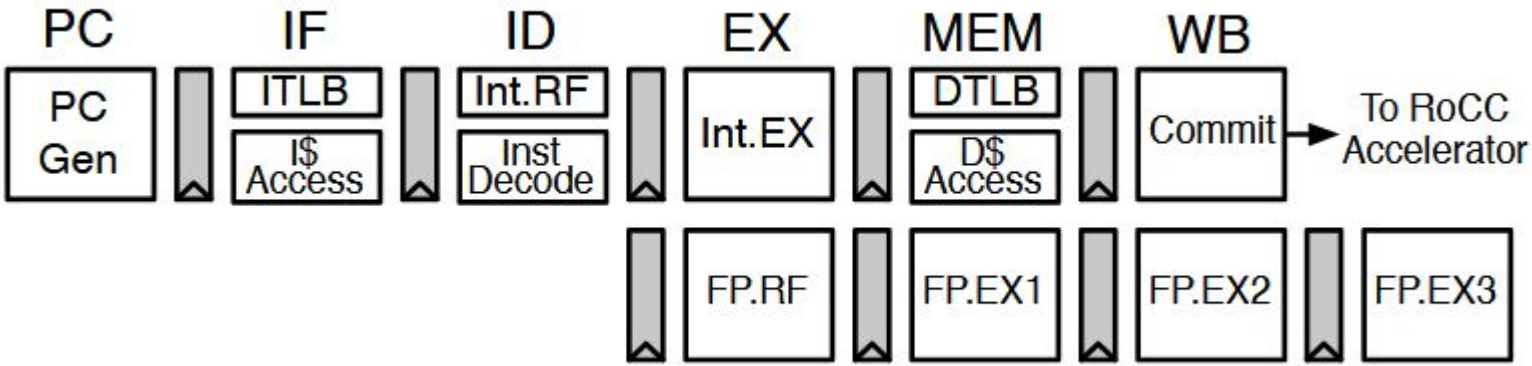
Rocket Core

- RV64GC
  - All of the extensions
- 5 stage pipeline
  - Separate multi-stage floating point pipeline
- Branch Prediction
  - Branch Target Buffer, Branch History Table, Return Address Stack

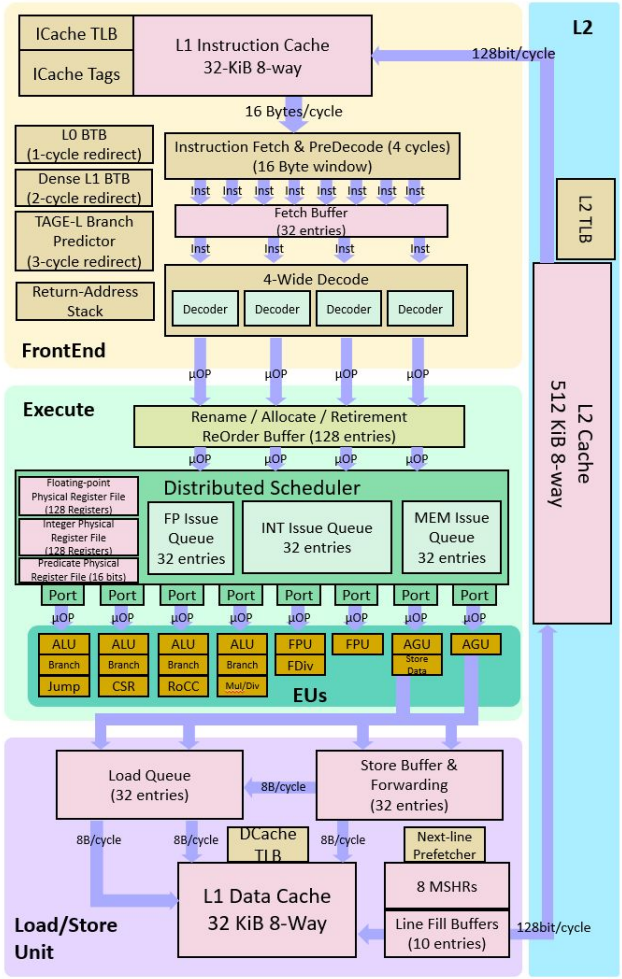
Submodule	Number of flip-flops
Register file	1,984
Control and status registers	984
Instruction buffer	76
Integer pipeline	872
Multiplier/Divider	214
Total	4,130



BOOM

- Berkeley's Out of Order Machine
  - Fetches 16 bytes at a time into window
  - Issues 4 instructions at a time
  - ~10 logical stages, broken up into 7 physical stage pipeline
- Boots Linux
  - TLB for virtual memory
  - Privileged Modes
- RV64GC

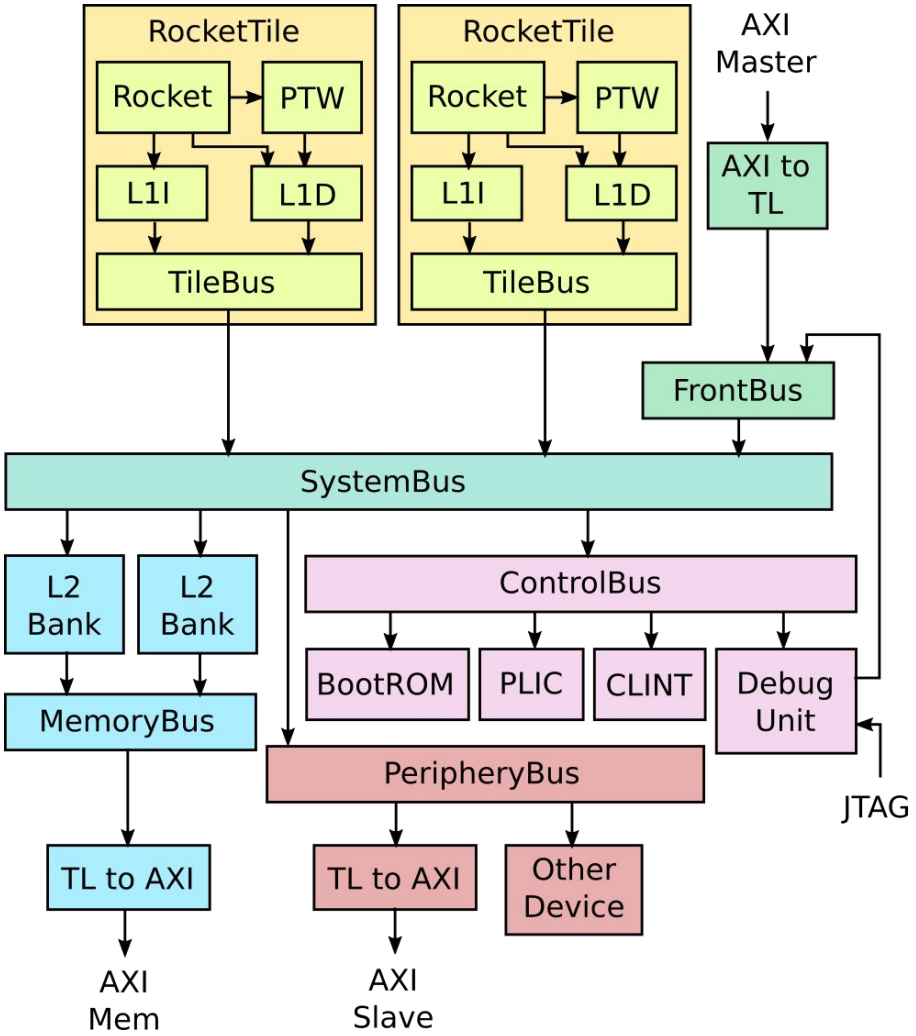
Submodule	Number of flip-flops
Register file	3,964
CSR	1,238
Instruction fetch	854
Register rename	1,547
Instruction issue	650
Load/Store unit	1,941
Arithmetic/logic unit	1,119
Reorder buffer	1,707
Branch prediction	465
Total	13,485



Rocket Chip: SoC Generator

- Automatically generate system on chip based on abstract config
- Uses its own TileLink (TL) protocol
  - Can be adapted to AXI

- Compatible with multiple cores
  - Rocket, BOOM, or any other TileLink adapted device
- Adaptable cache setup
  - Each core encompassed in tile with its own L1 cache
  - Shared L2 cache

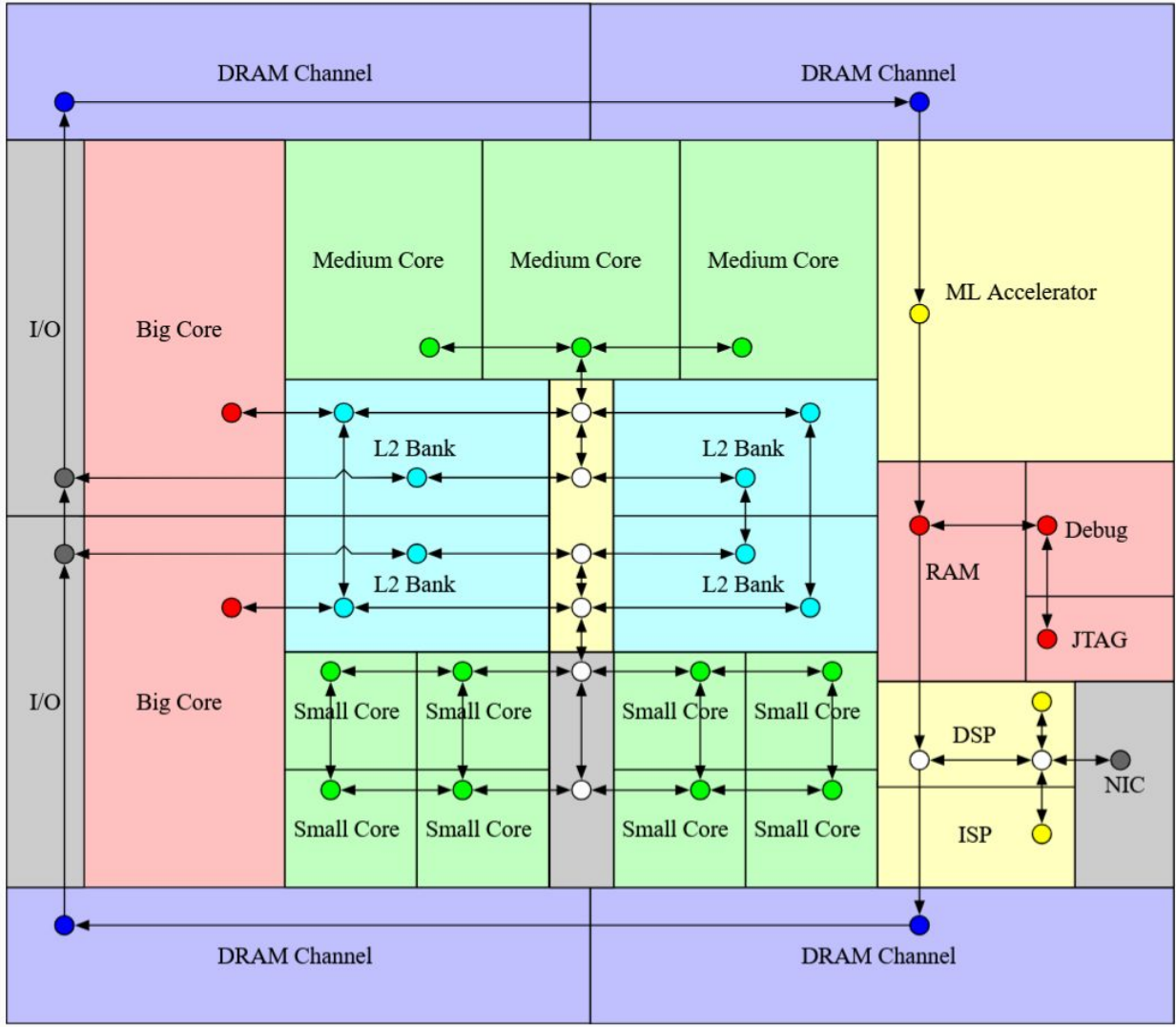


Constellation: NoC Generator

- Automatically generate network on chip
- Built for heterogeneous systems

- Uses directed graphs to define routing architecture
  - Supports arbitrary layouts

- Uses its own transport layer
  - Can transport AXI-4 or TileLink
- Flow Control



Honorable Mentions

- VexRiscv
  - Written in SpinalHDL
    - Another Scala-based HDL
  - 5+ Stage Pipeline
  - RV32I
    - Optional Multiply, Compressed, Atomic
    - Optional Float or Double
  - VexiiRiscv (successor) is RV64IMAFDCB
- CVA6
  - Written in System Verilog
  - 6 stage pipeline
  - RV64 IMAC, privilege modes

References

- https://chipyard.readthedocs.io/en/latest/index.html
- https://github.com/lowRISC/ibex
- https://github.com/olofk/serv
- https://github.com/YosysHQ/picorv32